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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,315	02/09/2004	Naoki Kuroda	60188-762	6654
7590	04/06/2005		EXAMINER	
Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY 600 Thirteenth Street, N.W. Washington, DC 20005-3096				NGUYEN, HAI L
		ART UNIT		PAPER NUMBER
		2816		

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,315	KURODA ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 27 May 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2,4,5,21-26 and 36 is/are rejected.
- 7) Claim(s) 3,6-20,27-35,37 and 38 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 09 February 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>09 February 2004</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “pulse signal generating circuit for generating and outputting a pulse signal for determining the propagation timing of the transmission signal, based on a clock signal for determining the propagation timing of the transmission signal”; in claims 21-26; must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show a pulse signal generating circuit for generating and outputting a pulse signal for determining the propagation timing of the transmission signal, based on a clock signal for determining the propagation timing of the transmission signal; a delay element block which includes at least one delay element and in which a delay is added to the transmission signal; and a fuse circuit which includes at least one fuse, the fuse being melted down based on the pulse signal and a transmission signal which has passed through the delay element block as described in the specification (page 6, lines 14-20). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claimed limitations that “a pulse signal generating circuit for generating and outputting a pulse signal for determining the propagation timing of the transmission signal, based on a clock signal for determining the propagation timing of the transmission signal”; “a delay element block which includes at least one delay element and in which a delay is added to the transmission signal”; and “a fuse circuit which includes at least one fuse, the fuse being melted down based on the pulse signal”, in claim 21, have not been enabled in the specification. The details of such functions are not seen in the description of the preferred embodiment. It is not clear as currently defined, how the instant invention can perform the recited functions.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 4, 5 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al. (US 6,202,168).

With regard to claim 1, Saito et al. discloses in Fig. 4 a semiconductor device comprising first and second circuit blocks (401, 408) provided on a semiconductor chip and including respective functional elements; and a timing adjustment circuit block (405 – 407) for adjusting a propagation timing of a transmission signal flowing on a line connecting the first and second circuit blocks to each other.

With regard to claim 2, the semiconductor device further comprises a comparison control circuit (413) for receiving an input signal (SYNC) input to the first circuit block and an output signal (Q2) output from the second circuit block which has received the transmission signal, comparing the input signal to the output signal, and controlling the timing adjustment circuit block.

With regard to claim 4, the reference also meets the recited limitations in the claim.

With regard to claim 5, the semiconductor device further comprises an input pattern generating circuit (414) for generating and outputting the input signal to the first circuit block.

With regard to claim 36, the second circuit block (408) is a memory circuit block (by given the broadest reasonable interpretation; the circuit block 408 is a memory circuit block because it has a function of storing a signal).

Allowable Subject Matter

8. Claims 3, 6-20, 27-35, 37 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 1), as recited in claim 3, having specific structural limitation such as the line (DAs) comprises a plurality of parallel lines (DA1, DA2 in instant Fig. 3), and each of the first and second circuit blocks (11 and 12 in instant Fig. 1,) includes a shift register (14, 15) connected to the plurality of lines, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 1), as recited in claim 11, having specific structural limitation such as the comparison control circuit (19) includes a control circuit (18) for outputting timing adjustment control signals (CNT) to the timing adjustment circuit block (13) when the comparison result shows that the input signal (16) and the output signal (OUT) differ from each other, the timing adjustment circuit block (13 in instant Fig. 3) includes a counter circuit (32) for receiving the timing adjustment control signals (CNT), and counting and electrically holding the number of the received timing adjustment control signals; a delay element block (31) which includes at least

one delay element and in which a delay amount depending on the number of the timing adjustment control signals is added to the transmission signal; and a fuse circuit (33) which includes at least one fuse and holds the number of the timing adjustment control signals in correspondence with the number of fuses which are melted down, wherein an output signal from the counter circuit or an output signal from the fuse circuit is selectively input to the delay element block, and the fuse is melted down based on the output signal from the counter circuit, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 1), as recited in claim 6, having specific structural limitation such as the timing adjustment circuit block (13 in instant Fig. 3) includes a first holding circuit (32, 33) for holding update information (CNT) in which the propagation timing of the transmission signal is updated, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 13), as recited in claim 27, having specific structural limitation such as the input pattern generating circuit (61, 62) for generating and outputting the input signal (IN2) to the first circuit block (11), wherein the input pattern generating circuit is activated when the comparison result (1) from the comparison control circuit (19) shows that the input signal and the output signal (OUT2) differ from each other, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 14), as recited in claim 32, having specific structural limitation such as the comparison control circuit (19) includes a control circuit (18) for outputting timing adjustment control signals (CNT) to the timing adjustment circuit block (13) when the comparison result shows that the input signal (IN2) and the output signal (OUT2) differ from each other, the timing adjustment circuit block (70 in instant Fig. 15) includes a counter circuit (32) for receiving the timing adjustment control signals, and counting and electrically holding the number of the received timing adjustment control signals; a delay element block (31) which includes at least one delay element and in which a delay amount depending on the number of the timing adjustment control signals is added to the transmission signal; and a nonvolatile memory circuit (71), wherein, an output signal from the counter circuit or an output signal from the nonvolatile memory circuit is selectively input to the delay element block, and the number of the timing adjustment control signals is written into the nonvolatile memory circuit based on the output signal from the counter circuit, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a semiconductor device (10 in instant Fig. 7), as recited in claim 37, having specific structural limitation such as the output timing changing circuit (43, 44 in instant Fig. 8) for changing the timing of outputting (DOUTD) an output signal (DOUT) from the memory circuit block in synchronization with a change of the propagation timing (42) of a clock signal (CLK to CLKD) for determining the propagation timing of the transmission signal (DAs), and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

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Conclusion

9. Regarding claims 21-26, the patentability thereof cannot be determined because of failing to comply with the enablement requirement.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN 
March 26, 2005



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